AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (ORIGINAL) A cache device set up in each of processors, interconnected to other cache devices in other processors and connected to a main memory, which comprises:

a cache memory wherein a part of data in the main memory is stored in one or more cache lines and a state tag using to manage data consistency is set up in each of the cache lines, and

a cache controller for carrying out, in the case that at the time of generation of a pre-fetch request following a read request from one of the processors the data stored in the other cache devices cannot be read unless its state tag is changed, weak read operation for causing failure in said pre-fetch request as a fetch protocol.

2. (ORIGINAL) The cache device according to claim 1, wherein said cache memory distinguishes the stored data by a data-modified state (M), an exclusive state (E), a data-shared state (S) and an invalid state (I), each of which indicates validity of the state tag, and

said cache controller causes failure in said pre-fetch request when the data corresponding to the pre-fetch request stored in the other cache devices is in the data-modified state (M) or the exclusive state (E).

3. (ORIGINAL) The cache device according to claim 1, wherein said cache controller reads, when the data corresponding to the pre-fetch request and stored in the other cache devices is in the invalid state (I), the same data from said main memory and stores the same data in the exclusive state (E) in the cache memory; and when the data is in the data-shared state (S), the cache controller reads the data from the other cache devices and stores the data in the data-shared state (S) in the cache memory.

4. (ORIGINAL) A cache device set up in each of processors, interconnected to other cache devices in other processors and connected to a main memory, which comprises:

a cache memory wherein a part of data in the main memory is stored in one or more

cache lines and a state tag using to manage data consistency is set up in each of the cache lines, and

a cache controller for carrying out a pre-fetch protocol that in the case that at the time of generation of a pre-fetch request following a read request from one of the processors the data stored in the other cache devices cannot be read without changing its state tag, the data is read without changing the state tag and stored in the cache memory with the setup of a weak state W, and at the time of synchronization operation of memory consistency to attain data-consistency by software the data in the cache memory in said weak state (W) is wholly invalidated.

5. (CURRENTLY AMENDED) The cache device according to claim ~~3~~1, wherein said cache memory distinguishes the stored data by a data-modified state (M), an exclusive state (E), a data-shared state (S) and an invalid state (I), each of which indicates validity of the state tag, and

said cache controller reads, when the data which corresponds to the pre-fetch request and are stored in the other cache devices is in the data-modified state (M) or the exclusive state (E), the data without changing the state tag and stores the data in the cache memory with the setup of the weak state (W), and at the time of synchronization operation of the memory consistency the cache controller changes the weak state (W) into the invalid state (I) wholly.

6. (ORIGINAL) The cache device according to claim 5, wherein said cache controller reads, when the data corresponding to the pre-fetch request and stored in the other cache devices is in the invalid state (I), the same data from said main memory and stores the same data in the exclusive state (E) in the cache memory; and when the data is in the data-shared state (S), the cache controller reads the data from the other cache devices and stores the data in the data-shared state (S) in the cache memory.

7. (CURRENTLY AMENDED) A cache device set up in each of processors, interconnected to other cache devices in other processors and connected to a main memory, which comprises:

a cache memory wherein a part of data in the main memory is stored in one or more cache lines and a state tag using to manage data consistency is set up in each of the cache lines, and

a cache controller for carrying out a pre-fetch protocol that at the time of generation of a pre-fetch request following a read request from one of the processors, a passive preservation mode P is set up to data pre-fetched from the other cache devices or the main memory, and then the data is stored in said cache memory; when the data corresponding to the read request from the other cache devices is the pre-fetch data to which said passive preservation mode P is set up, the other cache devices ~~is~~ are not informed of the preservation of the corresponding data; when none of the other cache devices store the corresponding data, said pre-fetch data is invalidated; and when the other cache devices share the corresponding data, said pre-fetch data is stored as it is.

8. (ORIGINAL) The cache device according to claim 7, wherein said cache memory distinguishes the stored data by a data-modified state (M), an exclusive state (E), a data-shared state (S) and an invalid state (I), each of which indicates validity of the state tag, and

in the case that the data corresponding to the read request from some other cache device is the pre-fetch data to which said passive preservation mode P is set up, said cache controller changes the pre-fetch data stored in the passive preservation mode P into the invalid state (I) when all of the other cache devices are in the invalid state (I), or either one of the other cache devices is in the data-modified state (M) or the exclusive state (E), and the cache device keeps the state of the pre-fetch data stored in the passive preservation mode P as it is when the other cache devices are in the data-shared state (S).

9. (ORIGINAL) The cache device according to claim 7, wherein a normal preservation mode N is set up to data other than the pre-fetch data in the passive preservation mode P stored in said cache memory, and data-preservation in the passive preservation mode P and data-preservation in the normal preservation mode N are carried out in the respective cache lines, and caused to exist together.

10. (CURRENTLY AMENDED) The cache device according to claim ~~1~~ 4, wherein said cache controller carries out, when the cache controller receives the read request from said processor, a pre-fetch request for pre-fetching data in one or more addresses adjacent to a read-requested address after said read request.

11. (PREVIOUSLY PRESENTED) The cache device according to claim 1, wherein

said cache controller carries out, when the cache controller receives the read request from said processor, a pre-fetch request for pre-fetching data in one or more addresses adjacent to a read-requested address after said read request.

12. (CURRENTLY AMENDED) The cache device according to claim 11, wherein ~~said interconnecting network is~~ the cache device is interconnected to the other cache devices via a snoop bus for outputting, when said cache controller receives a read request from its own processor or some other cache devices, ~~the~~ preservation states of the corresponding data into state controlling lines; the state controlling lines are a state controlling line which corresponds to and is exclusive for the read request and a state controlling line which corresponds to and is exclusive for a pre-fetch request, the read request and the pre-fetch request being carried out by said cache controller at the same time; and the states of the respective cache devices about the an address of the requested data and an address of the pre-fetch requested data are conveyed at the same time.

13. (ORIGINAL) The cache device according to claim 11, wherein in response to the simultaneous requests of said read request and the pre-fetch request, a distinguishing bit for distinguishing data in response to said read request and data in response to the pre-fetch request is fitted up to a response header, and data making the distinguishing bit valid are transmitted in a lump.

14. (CURRENTLY AMENDED) A method for controlling a cache system wherein cache devices set up in respective processors are mutually connected through an interconnecting network and are connected to a main memory,

which comprises ~~the steps of~~:

storing a part of data in the main memory in one or more cache lines on cache memory and setting up a state tag using to manage data consistency in each of the cache lines, and

carrying out, in the case that at the time of generation of a pre-fetch request following a read request from one of the processors data stored in the other cache devices cannot be read unless its state tag is changed, weak read operation for causing failure in said pre-fetch request as a fetch protocol.

15. (CURRENTLY AMENDED) A method for controlling a cache system wherein cache devices set up in respective processors are mutually connected through an interconnecting network and are connected to a main memory,

which comprises ~~the steps of~~:

storing a part of data in the main memory in one or more cache lines on cache memory and setting up a state tag using to manage data consistency in each of the cache lines,

reading, in the case that at the time of generation of a pre-fetch request following a read request from one of the processors the data stored in the other cache devices cannot be read without changing its state tag, the data without changing the state tag to respond to said processor, and subsequently storing the data, with the setup of a weak state W, in the cache memory, and

invalidating, at the time of synchronization operation of memory consistency to attain data-consistency by software, the data in the cache memory in said weak state (W) wholly.

16. (CURRENTLY AMENDED) A method for controlling a cache system wherein cache devices set up in respective processors are mutually connected through an interconnecting network and are connected to a main memory,

which comprises ~~the steps of~~:

storing a part of data in the main memory in one or more cache lines on cache memory and setting up a state tag using to manage data consistency in each of the cache lines,

setting, at the time of generation of a pre-fetch request following a read request from one of the processors, a passive preservation mode P to data pre-fetched from the other cache devices or the main memory and storing the data in said cache memory,

not informing, when data corresponding to the read request from the other cache devices is the pre-fetch data to which said passive preservation mode P is set, the other cache devices of preservation of the corresponding data, and

invalidating said pre-fetch data when none of the cache devices store the corresponding data, and storing said pre-fetch data as it is when the corresponding data is shared by the other cache devices.